

CMOS Image Sensor Architecture for Primal-Dual Coding

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Abstract—A CMOS image sensor architecture for primal-dual coding (PDC), the developed image sensor and the sensing side of the system, as well as preliminary sensor test results are presented in this paper. The architecture proposed in this work uses pixels with the embedded 2-bit latches which are responsible for the pre-loading and storing of the exposure codes. The subsequent exposure code (mask) can therefore be loaded while the current mask is being used for exposure, resulting in a pipelined coding operation which does not interfere with the pixel exposure time. The mask loading is done serially via a vertical metal line (one line per-column), making both the imager architecture and the pixel array scalable towards high pixel resolutions. The sensor is designed using a $0.35\mu\text{m}$ image sensor optimized CMOS process resulting in the total pixel pitch of $25\mu\text{m}$. The pixel includes a photo-gate based photodetector, two 1-bit latches, required logic gates, two charge collection buckets (floating diffusions) and corresponding symmetric readout with two source-followers (one for each bucket), resulting in a pixel fill-factor of 20.5%. Every pixel column features a programmable gain amplifier whose outputs are time-multiplexed over 3 analog output pads. Analog-to-digital conversion is performed off-chip by 3×16 -bit ADCs. The 60×80 pixel imager consumes 7mW of power while operating at 25 fps. The sensor measurement results show that the loading of the complete PDC mask for the whole array can be performed in $30\mu\text{s}$, resulting in a large number of masks that can be applied during a single exposure time, therefore creating a very promising platform for an effective and optimal use of PDC.

I. INTRODUCTION

Primal-dual-coding (PDC) refers to an active illumination technique where coding is applied to both the light emission at the source (the primal domain) and light detection on the sensor side (the dual domain). To acquire an image, a sequence of 2D patterns is projected onto the scene, while another sequence of 2D mask patterns is applied in lockstep to control sensor's exposure. Previous research in computational imaging has shown that PDC is a very effective tool in actively probing light transport and can therefore provide many potentially interesting imaging capabilities such as separating direct and indirect light paths based on the number of reflections, eliminating scattered light, improving

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the accuracy and/or power efficiency of structured light and other 3D imaging systems [1]–[4]. However, performing light transport probing in the optical domain typically results in a large, unportable and expensive optical system [4]. Hence, to fully exploit the potential benefits of the scheme, an electrical implementation of the selective light sensing is required which in turns needs a customized image sensor architecture capable of arbitrarily coding the pixel exposure in both spatial and time domain. Coded-exposure imaging has previously found use in applications such as compressive sensing [5], [6], motion deblurring [7]–[9], and high-speed imaging [10] where the coded-exposure pixels are used to eliminate the effects of rolling shutter.

The sensor architecture proposed in this work uses pixels with the embedded latches which are responsible for the pre-loading and applying the exposure codes. The subsequent exposure code (mask) can therefore be loaded while the current mask is being used for exposure, resulting in a pipelined coding operation which does not interfere with the pixel exposure time. The mask loading is done serially via a vertical metal line (one line per-column), making both the imager architecture and the pixel array scalable towards high pixel resolutions.

II. CODED-EXPOSURE PIXELS

The sensing side of the PDC scheme requires arbitrary pixel masking in order to selectively choose the desired light paths. Depending on the information/application of interest, these masks can take very different shapes and need to change many times during a single image frame exposure (see Figure 1(a) for simple examples). In order to electrically implement this functionality, the complete frame exposure time is divided into many different “subframes” and a single bit of data is sent to each individual pixel to define the value of the pixel mask during the corresponding subframe. The pixel has two photon-electron collection nodes (buckets). Depending on whether the pixel masking bit value is one or zero (see Figure 1(b)), the signal is either integrated on the first or on the second bucket, respectively.

Having two buckets allows the sensor collect the signal even when the pixel is masked by the PDC scheme. Besides allowing more useful signal to be collected (without wasting any of the active light), having two buckets is especially useful in applications such as direct and indirect light separation, since both the direct and indirect light path signal-related charges can be collected (and separated) during the complete frame exposure time.

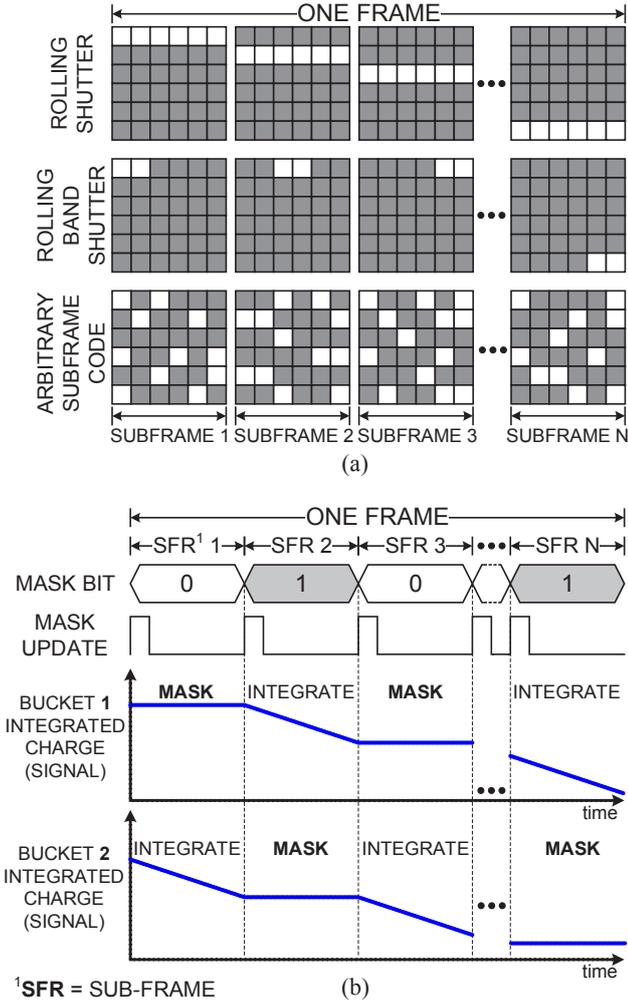


Figure 1. An illustration of the electrical coded-exposure implementation: (a) coded-exposure imaging examples of the typical PDC masks that could be applied over many different subframes, (b) pixel timing diagram of the related pixel signal integration process depending on the masking bit value over multiple subframes.

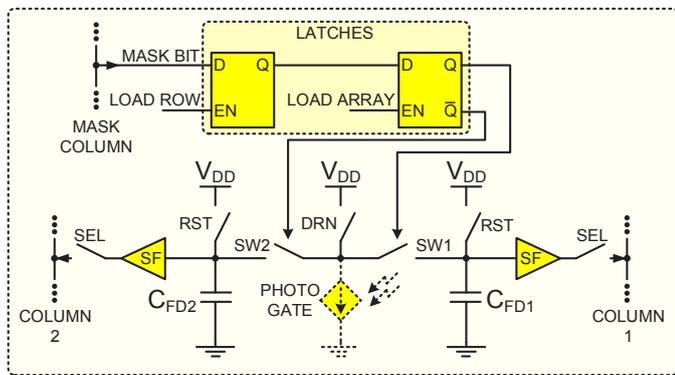


Figure 2. The proposed PDC pixel circuit diagram with level-sensitive latches.

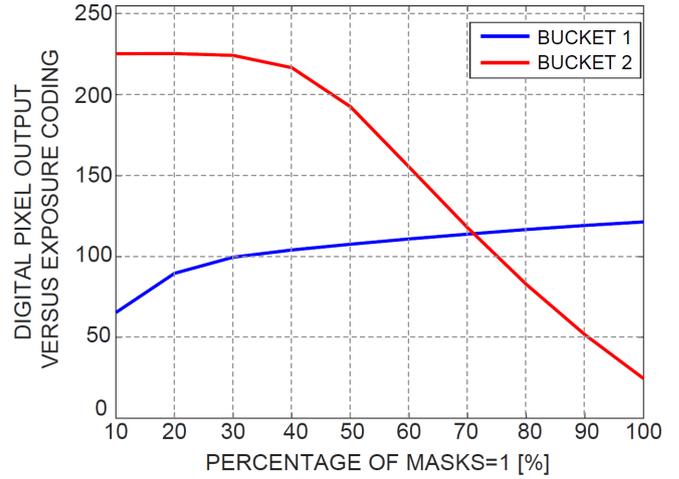


Figure 3. The measured digital pixel output at uniform light versus the coded pixel exposure expressed as percentage of masks applied over the complete frame exposure.

The coded-exposure pixel schematic is shown in Figure 2. Switches SW1 and SW2 are used to steer the collected charge towards the appropriate bucket depending on the latched mask bit value. Moreover, since one of the switches is kept on during the readout, the channel capacitance of the switch modulates the overall floating diffusion capacitance. This allows the pixel to intrinsically have a different conversion gain in two buckets. For direct and indirect light collection, this is an important feature because usually direct light has a significantly higher power than the indirect light. The difference in conversion gains depending on the pixel exposure coding is shown in Figure 3.

The pixel contains two level-sensitive latches. The first latch is used to memorize the mask bit (mask bit signal is routed vertically and is physically the same for the single column) when the corresponding LOAD ROW trigger signal arrives (the whole row of masks is loaded at the same time). The masks are loaded serially through 4 separate channels and the bits are then deserialized into a parallel data, i.e. 1-bit per every individual column. Once all the masks are loaded for all the 80 rows individually, the complete mask for the full frame is latched by the second latch. This mask loading process for a single subframe is illustrated in Figure 4. The same process is then repeated many times for every subframe within a single frame. Two latches allow for the light exposure of the current subframe while the exposure mask for the next subframe is being loaded row-by-row. This results in pipelining the operation of the mask deserialization and loading with the regular pixel operation.

III. SENSOR ARCHITECTURE

The complete sensor architecture is shown in Figure 5. Mask deserializing and timing circuit is placed on top of the pixel array. Pixel outputs are delta-double-sampled and amplified by the programmable-gain amplifiers and multiplexed over 3 analog output pads. Counting the dummy pixels and considering each pixel has two outputs, 46 pixel outputs (in total)

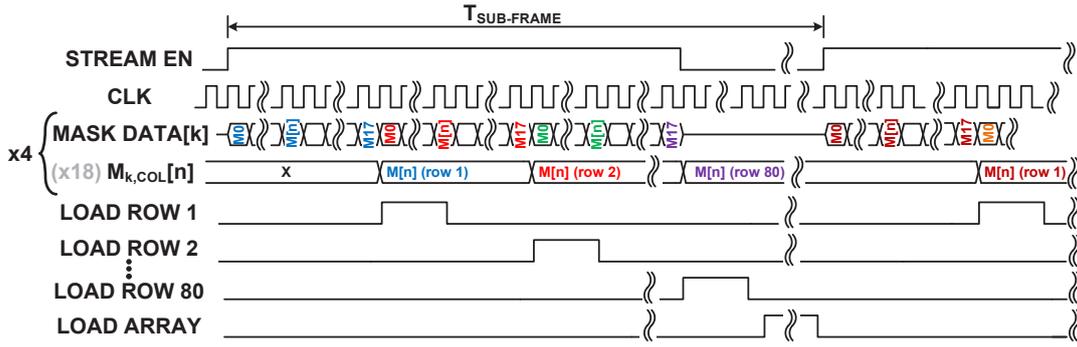


Figure 4. A simplified waveform diagram of the mask deserialization and loading.

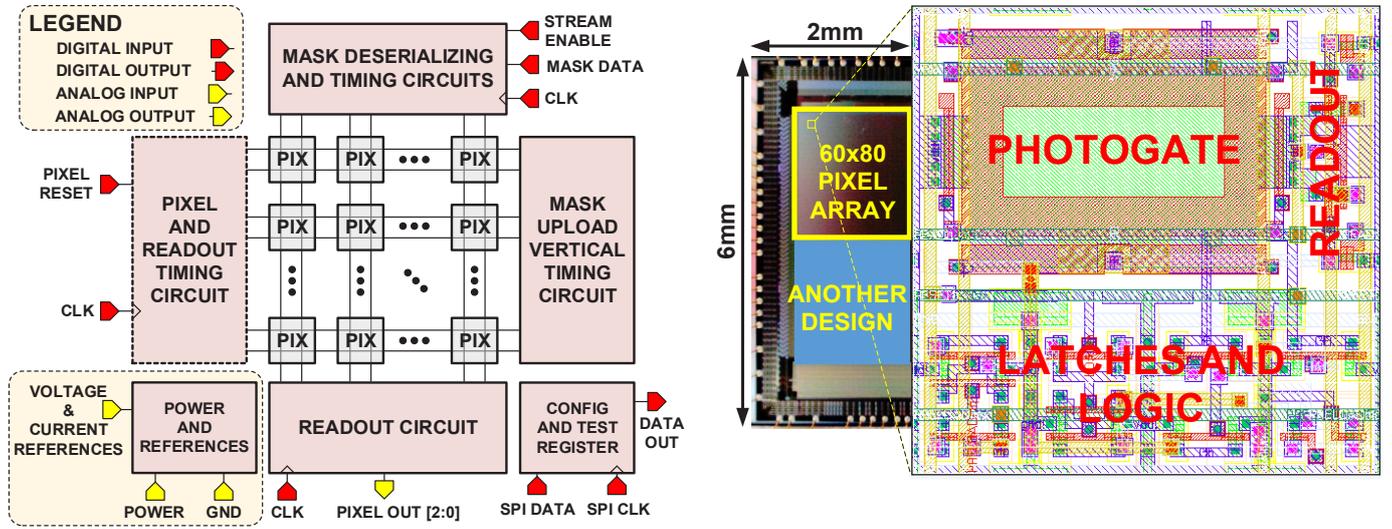


Figure 5. The proposed PDC CMOS image sensor architecture.

are multiplexed over each pad. Analog-to-digital conversion is performed off-chip by three 16-bit ADCs. The proposed pixel pitch is $25\mu\text{m}$ with the 20.5% fill-factor in the $0.35\mu\text{m}$ image sensor optimized CMOS process used in this work. The total resolution of the sensor is 60×80 pixels (see Figure 6).

IV. MEASUREMENT RESULTS

The results of coded-exposure imaging with the proposed design are shown in Figure 7. The complete system with the sensor (see Figure 8) is used to capture a photo of Lena shown on a computer screen. The sensor light exposure in Figure 7 is modulated by the number of masks equal to one (or zero) during a single image frame exposure time, and the outputs of both buckets are shown. From left to right, the number of mask bits equal to 0 gradually increases, showing how the bucket 1 gets unblocked and starts collecting more charge. Conversely, bucket 2 collects the signal initially, but starts being blocked more as the number of masking bits equal to zero increases (see also Figure 1). Based on the measurement results, the loading of the complete mask can be performed in $30\mu\text{s}$, allowing a relatively high number of masks to be applied during a single image frame.

Figure 6. The pixel layout and the image sensor die micrograph showing the chip region dedicated to PDC.

V. CONCLUSION

A prototype CMOS image sensor for primal-dual coding and the preliminary sensor test results are presented in this work. The sensor uses an in-pixel 2-bit memory to implement pipelined mask loading and coded-exposure. storing of the exposure codes. The sensor consumes 7mW of power from a 3.3V power supply, while operating at 25 fps frame rate. An investigation of the sensor's performance when used in combination with the active illumination (full PDC) system is yet to be fully conducted.

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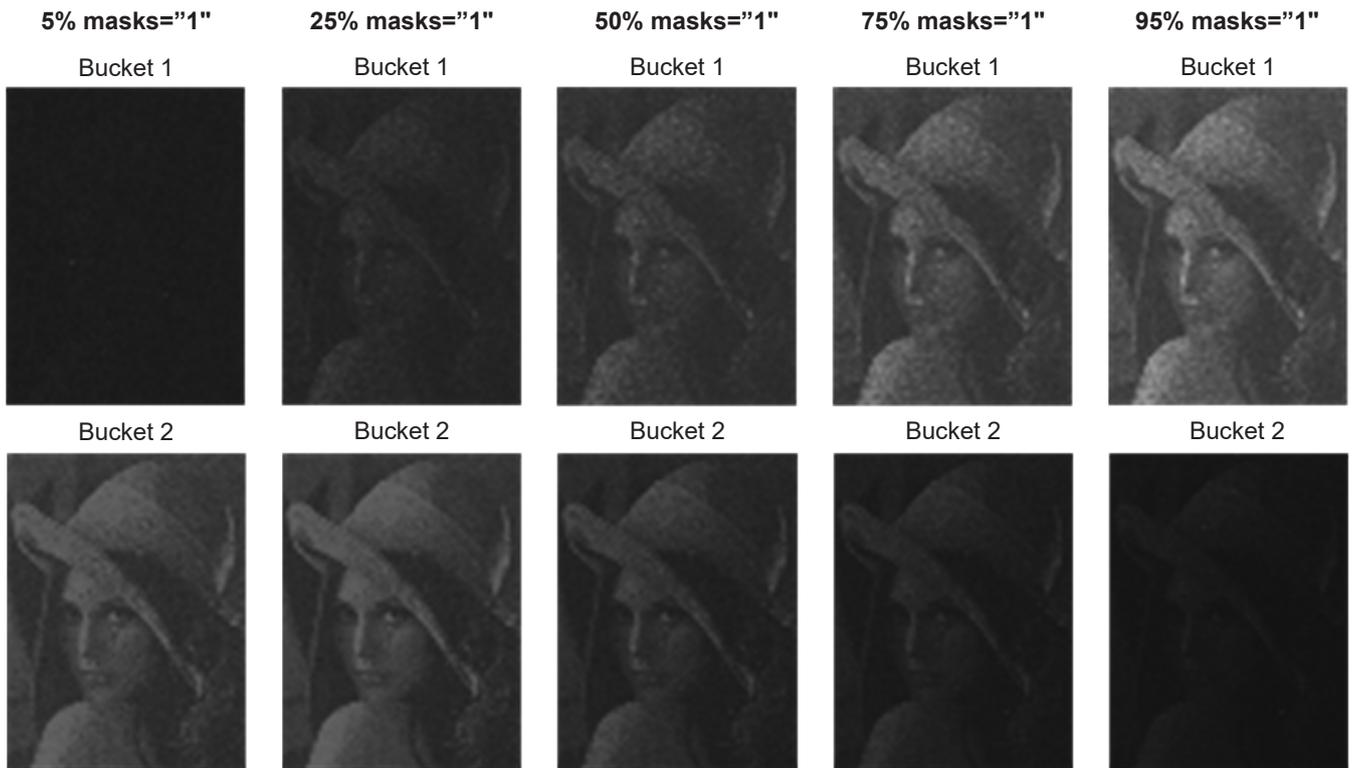


Figure 7. Capturing a photo of Lena shown on the computer screen, while changing the level of pixel masking. The number of masks equal to one starts from 5% on the left, and increases all the way up to 95% on the right. The output image is shown for each of the buckets.

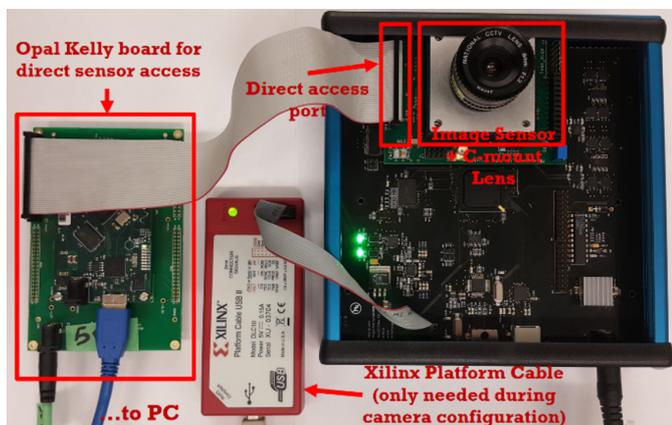


Figure 8. The complete sensing side of the imaging system with the camera system and the FPGA board used for the direct signal acquisition.

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