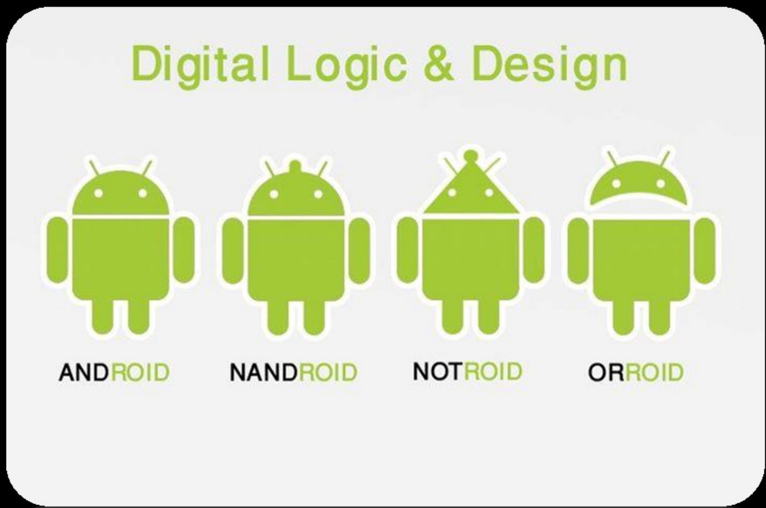
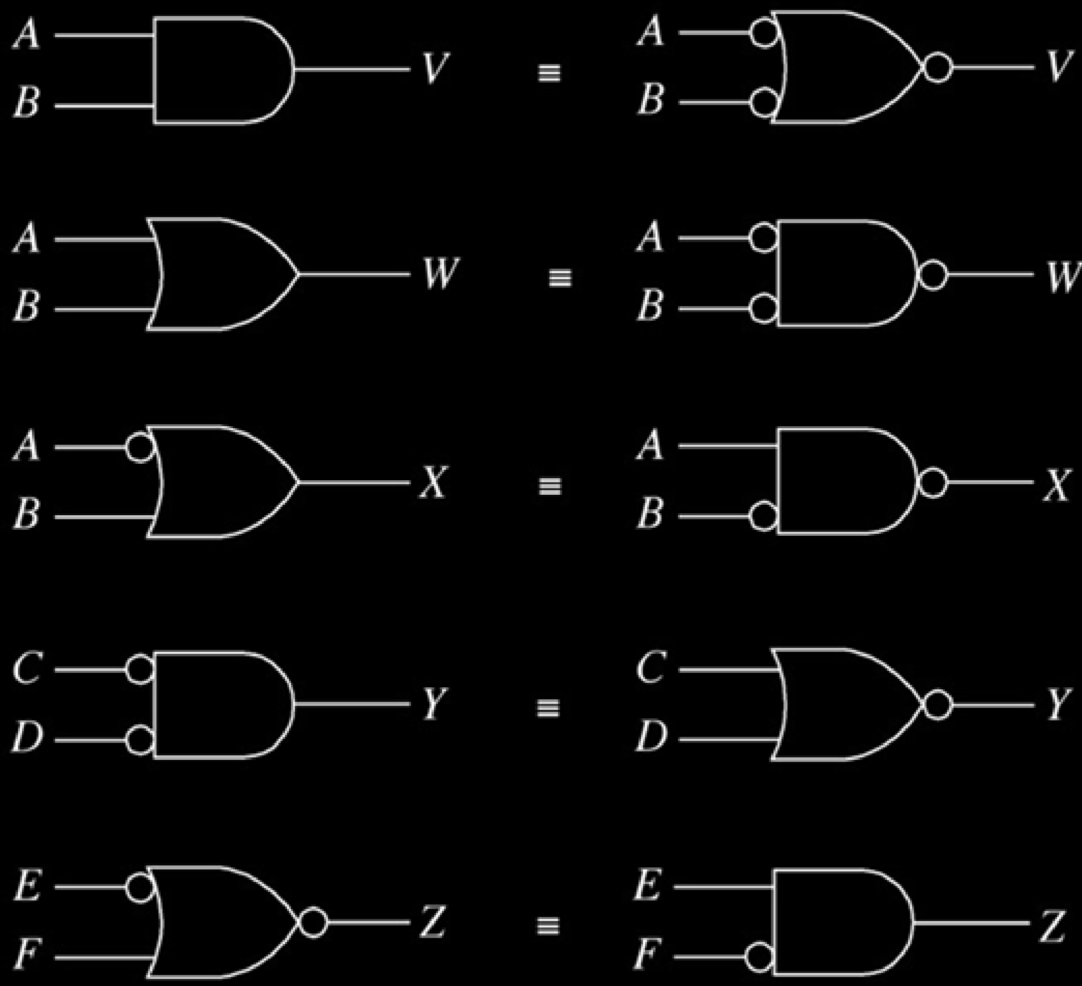
Week 2 & 3 Review

Review of past lecture:

- Last week we learned:
- Using logic gates
  - Combinational circuits
  - Circuit reduction
  - Karnaugh maps
- Logical Devices
  - Multiplexer
  - Decoder
  - Adder/Subtractor
  - Comparator



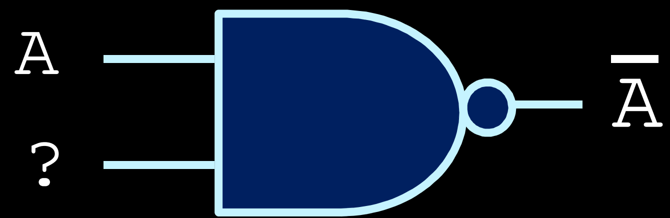
Gate Conversions

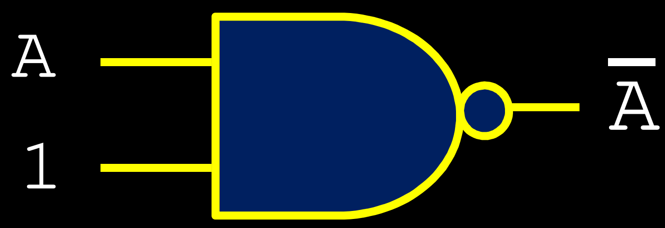


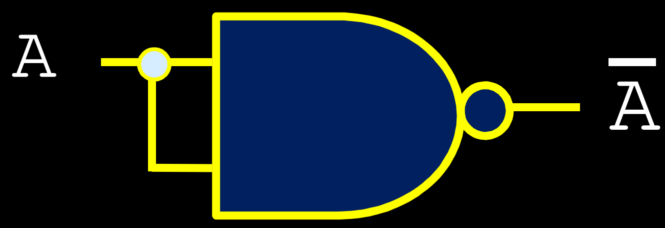
Quiz 3

Question 1

- How can you implement a NOT gate from a 2-input NAND gate?







Question 2 - Minterms

- Write Y in SOM (Sum Of Minterms) form.

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$Y = \overline{A} \cdot \overline{B} \cdot C + \overline{A} \cdot B \cdot \overline{C} + A \cdot \overline{B} \cdot \overline{C} + A \cdot B \cdot C$$

$$Y = m_1 + m_2 + m_4 + m_7$$

Question 3 - Maxterms

- Write Y in POM (Product Of Maxterms) form.

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$Y = \overline{A}+\overline{B}+C \cdot \overline{A}+B+\overline{C} \cdot \\ A+\overline{B}+\overline{C} \cdot A+B+C$$

$$Y = M_0 \cdot M_3 \cdot M_5 \cdot M_6$$

Question 4

Given the Karnaugh map on the right for an output called Y, what is the equation for **the most reduced form** of this circuit.

$Y = B' + D'$

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	0	0	1
11	1	0	0	1
10	1	1	1	1

Question 5

Given the Karnaugh map on the right for an output called Y:

a. **Gate Cost: ____1________________**

b. **Gate Cost (including NOTs) :__3________________**

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	0	0	1
11	1	0	0	1
10	1	1	1	1

Practice Question

- Given the minterms below, can you fill in the truth table on the right?

$$Y = m_2 + m_3 + m_7 + m_9 + m_{12} + m_{14}$$

A	B	C	D	Y
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Practice Question

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A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Question 6-8

6. How do you write the number 78 as an 8-bit binary number?

128	64	32	16	8	4	2	1
0	1	0	0	1	1	1	0

7. What is the two's complement of 01101101?

10010011

Tip for 2's comp:
preserve the first '1' and invert

8. What is the sum of 01101101 and 01101101?

11011010

Note what's happening here!

Question 9

- What groupings are in the K-map on the right?

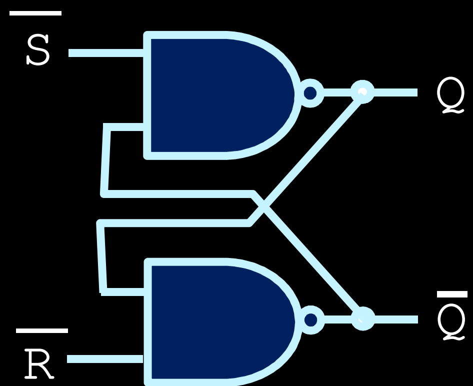
	$\overline{C}\cdot\overline{D}$	$\overline{C}\cdot D$	$C\cdot D$	$C\cdot\overline{D}$
$\overline{A}\cdot\overline{B}$	1	1	X	1
$A\cdot\overline{B}$	X	0	X	1
$A\cdot B$	1	X	X	1
$\overline{A}\cdot B$	1	X	0	X

- What logic equations do these groupings represent?

$$\overline{A}\cdot\overline{B} + \overline{D}$$

Question 10

Which Row is the forbidden state for this circuit?



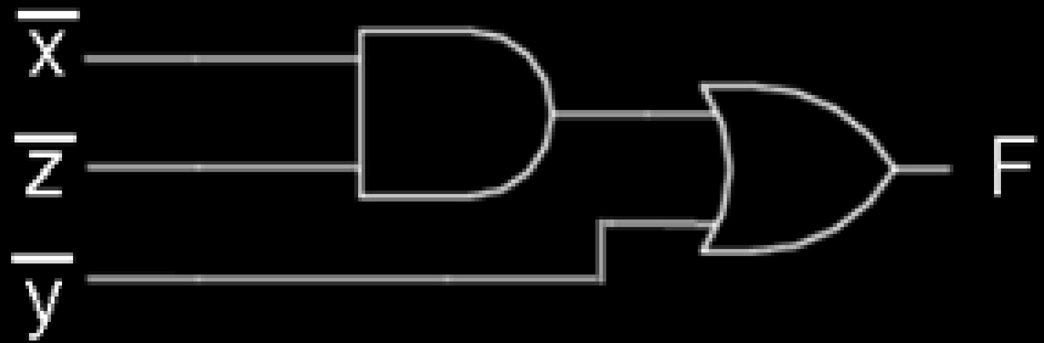
Row	$\overline{S}$	$\overline{R}$	Q_T	$\overline{Q}_T$	Q_{T+1}	$\overline{Q}_{T+1}$
A	0	0	X	X	1	1
B	0	1	X	X	1	0
C	1	0	X	X	0	1
D	1	1	0	1	0	1
E	1	1	1	0	1	0

Row A

Group Questions

Question 1

What is the Sum of Minterms equation for the circuit shown below:

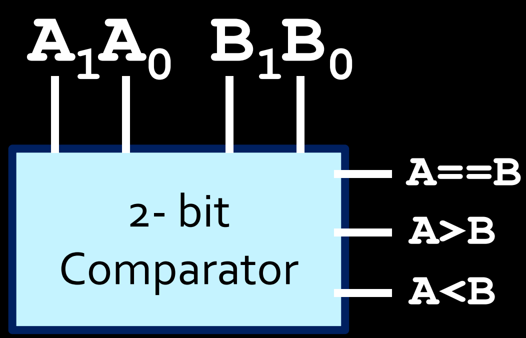


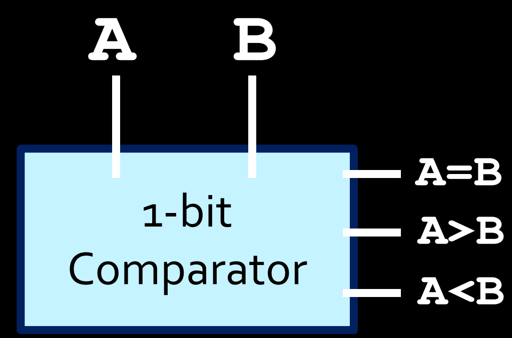
$F = m_0 + m_1 + m_2 + m_4 + m_5$

$F = \sum m\,(0,1,2,4,5)$

Question 2

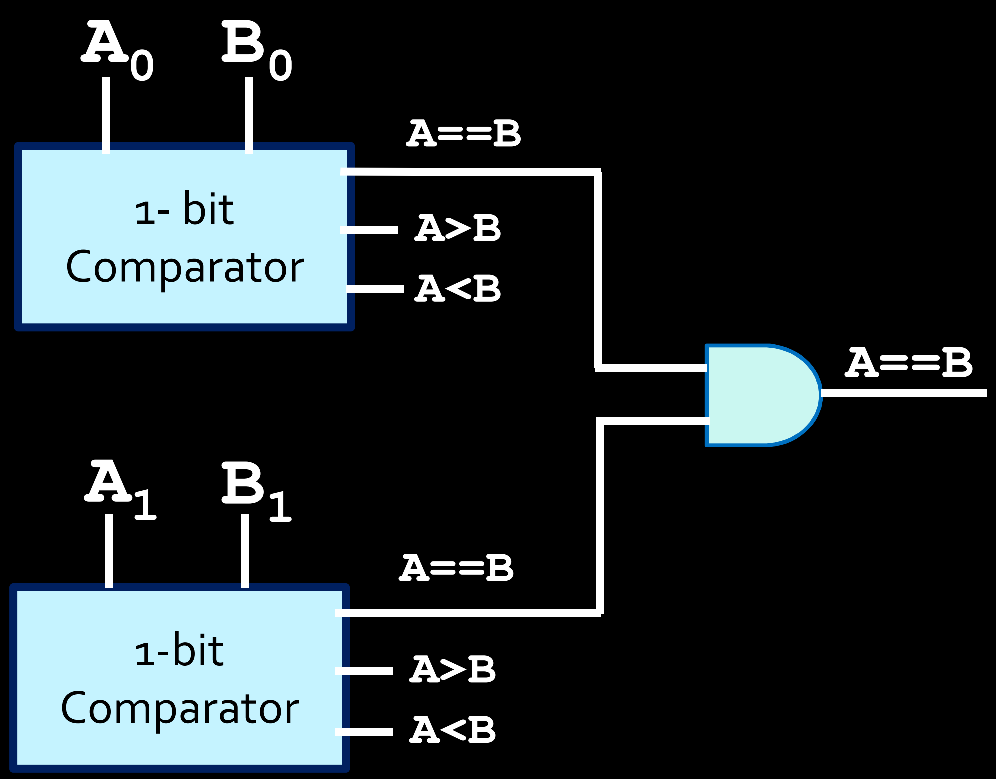
- How would you implement the A==B output of the 2-bit comparator below out of 1-bit comparators and a minimal number of gates?





Question 2 - Answer

- The implementation of the A==B signal:



Question 3

- How would you implement the A>B output of the 2-bit comparator below out of 1-bit comparators and a minimal number of gates?