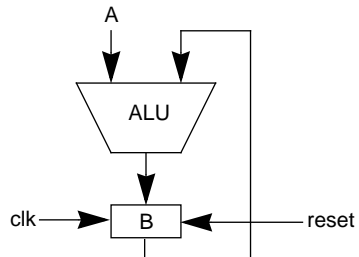


**CSC258 2002 Fall: Computer Organization**  
**Department of Computer Science, University of Toronto**  
**Lab 2 - ALU's and Sequential Circuits**

### 1. Arithmetic Logic Unit (ALU)

Gating and data transfer operations of a typical ALU will be studied using the structure shown in the block diagram below, which consists of a register (B) and an ALU.



Consider an ALU that consists of an n-bit adder. In order to add two operands, one of them must first be stored in register B. This is done by clearing register B so it contains zeros and then applying the operand at the external input (A). As a result, the output of the ALU will be equal to the operand at A. This operand can now be loaded into register B by clocking it. The second operand is then made available at A, an addition performed and the sum appears at the output of the adder.

Build and test the circuit using a 4-bit full adder chip (74LS283) and a 4-bit edge-triggered register (74LS175). Does the register need to be edge-triggered for this design, or would a level-sensitive flip-flop also work? Why?

### 2. Sequential Circuits

An electronic controller for an automatic transmission is to be designed. The transmission has 4 gears labelled using binary code as **00** (first), **01** (second), **10** (third) and **11** (fourth). Various sensors check driving conditions and generate two binary signals: **UP** and **DOWN**. Synchronization signal **CK** changes from 1 to 0 when levels on lines **UP** and **DOWN** are ready. Following are the specifications for operating the transmission:

- when **UP** = **DOWN** = 0 the transmission should remain in the same gear.
- when **UP** = 1 and **DOWN** = 0 the transmission should shift up by one gear.
- when **UP** = 0 and **DOWN** = 1 the transmission should shift down by one gear.
- combination **UP** = **DOWN** = 1 does not occur.
- any attempt to shift up while in fourth gear, or shift down while in first gear should result in no change of gears.

Design, build and test a synchronous sequential circuit that generates a gear number as a function of the current gear and the two control signals **UP** and **DOWN**. Use JK flip-flops, NAND gates and inverters. Your design should include a state diagram, state table, excitation table, simplified flip-flop input functions and circuit diagram