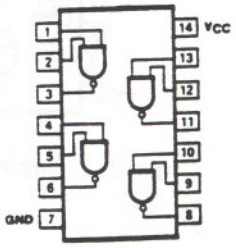
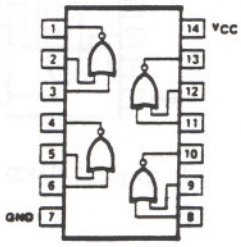
Pin out and Description of TTL Chips

74LS00



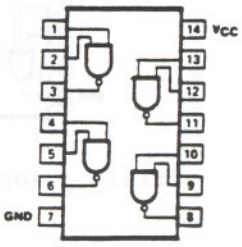
quad 2 input NAND gate

74LS02



quad 2 input NOR gate

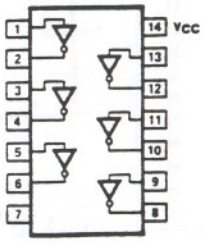
74LS03



quad 2 input NAND gate

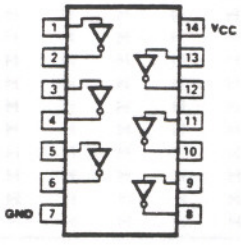
(open collector)

74LS04



hex inverters

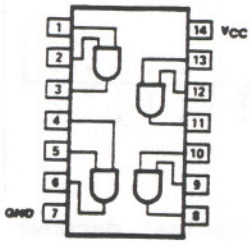
74LS05



hex inverters

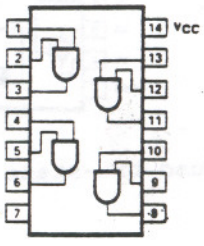
(open collector)

74LS08



quad 2 input AND gate

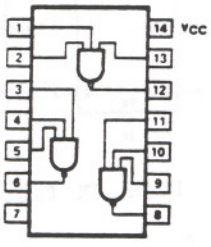
74LS09



uad 2 input AND gate

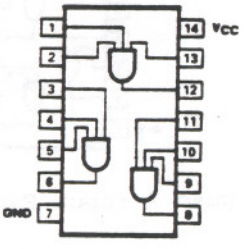
(open collector)

74LS10



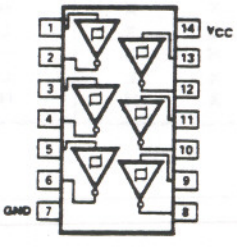
triple 3 input NAND gate

74LS11



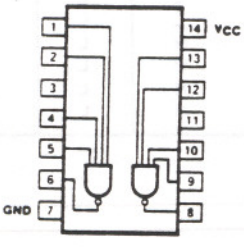
triple 3 input AND gate

74LS14



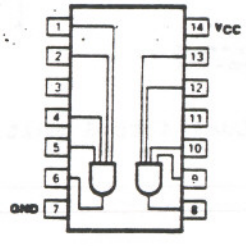
hex Schmitt trigger

74LS20



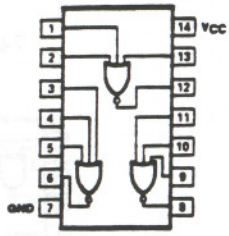
dual 4 input NAND gate

74LS21



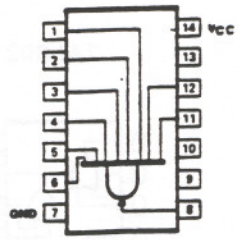
dual 4 input AND gate

74LS27



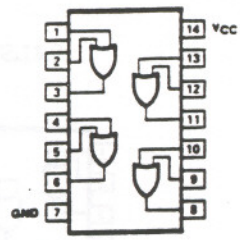
Triple 3 input NOR gate

74LS30



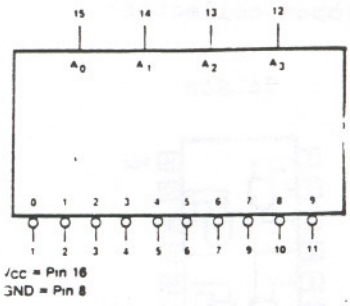
8 input NAND gate

74LS32



quad 2 input OR gate

74LS42



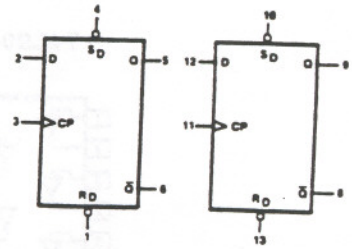
Vcc = Pin 16
GND = Pin 8

BCD to decimal decoder

TRUTH TABLE

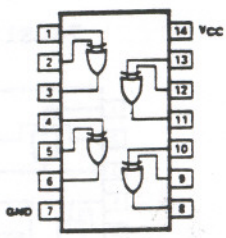
A_3	A_2	A_1	A_0	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$
L	L	L	L	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
L	H	H	H	H	H	H	H	H	H	H	L	H	H
H	L	L	L	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
H	L	H	L	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

74LS74



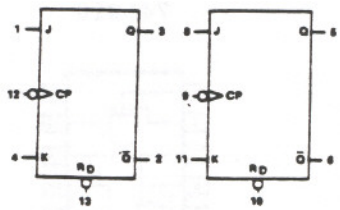
dual D type flip flop

74LS86



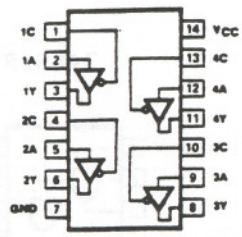
Quad 2 input Exclusive OR

74LS107



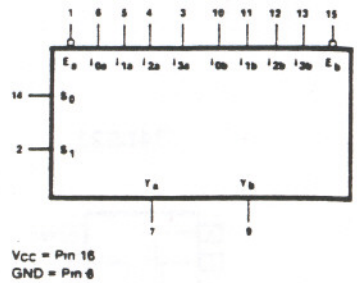
Dual JK flip flop

74LS125



quad tri-state buffers

74LS153



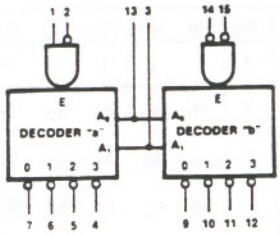
Vcc = Pin 16
GND = Pin 8

Dual 4 to 1 multiplexer

TRUTH TABLE

SELECT INPUTS		INPUTS (a or b)					OUTPUT
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	Y
X	X	H	X	X	X	X	L
L	L	L	L	X	X	X	L
L	L	L	H	X	X	X	H
H	L	L	X	L	X	X	L
H	L	L	X	H	X	X	H
L	H	L	X	X	L	X	L
L	H	L	X	X	H	X	H
H	H	L	X	X	X	L	L
H	H	L	X	X	X	H	H

74LS155



V_{CC} = Pin 16
GND = Pin 8

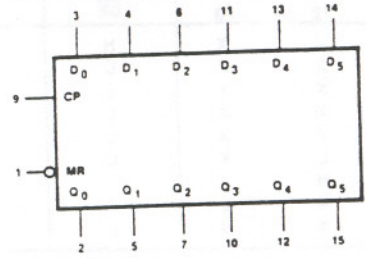
TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
A_0	A_1	E_a	$\overline{E}_a$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{E}_b$	$\overline{E}_b$	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care.

dual 2 of 4 decoder/multiplexer

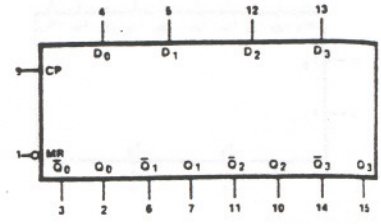
74LS174



V_{CC} = Pin 16
GND = PIN 8

hex D type flip flop with reset

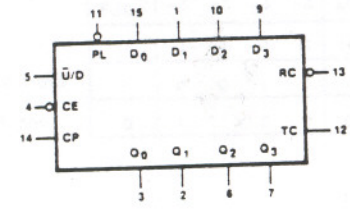
74LS175



V_{CC} = Pin 16
GND = Pin 8

quad D type flip flop with reset

74LS191



V_{CC} = Pin 16
GND = Pin 8

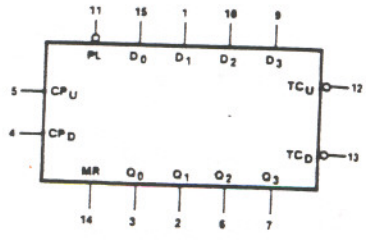
4 bit binary up/down counter

TC AND $\overline{RC}$ TRUTH TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	X	X	H	H	H	H	L	H
L	H	X	H	H	H	H	H	H
L	L	⊓	H	H	H	H	H	⊓
L	X	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊓	L	L	L	L	H	⊓

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
I = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
X = Don't care.
↓ = LOW-to-HIGH clock transition.
⊓ = LOW pulse.

74LS193



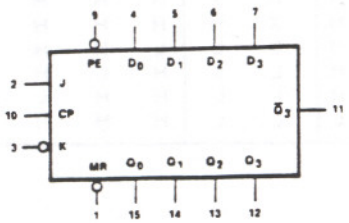
V_{CC} = Pin 16
GND = Pin 8

4 bit binary up/down counter

MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS		
	MR	$\overline{PL}$	CP_U	CP_D	D_0,D_1,D_2,D_3	Q_0,Q_1,Q_2,Q_3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X X X X	L L L L	H	L
	H	X	X	H	X X X X	L L L L	H	H
Parallel load	L	L	X	L	L L L L	L L L L	H	L
	L	L	X	H	L L L L	L L L L	H	H
	L	L	L	X	H H H H	H H H H	L	H
	L	L	H	X	H H H H	H H H H	H	H
Count up	L	H	↑	H	X X X X	Count up	H(b)	H
Count down	L	H	H	↑	X X X X	Count down	H	H(c)

74LS195



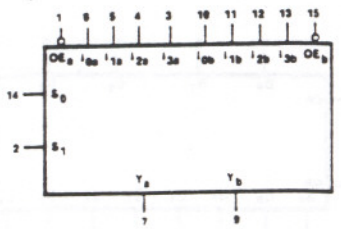
V_{CC} = Pin 16
GND = Pin 8

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS						OUTPUTS				
	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	↑	h	h	h	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	↑	h	l	l	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	↑	h	h	l	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	↑	h	l	h	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	↑	l	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

4 bit parallel access shift register

74LS253



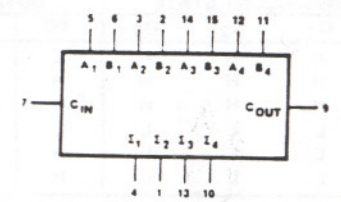
V_{CC} = Pin 16
GND = Pin 8

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT ENABLE	OUTPUT
S_0	S_1	I_0	I_1	I_2	I_3	$\overline{OE}$	Y
X	X	X	X	X	X	H	(Z)
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
H	L	X	L	X	X	L	L
H	L	X	H	X	X	L	H
L	H	X	X	L	X	L	L
L	H	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

dual tri-state 4-1 multiplexer

74LS283

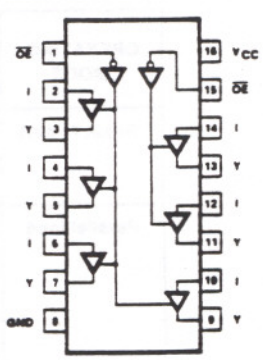


V_{CC} = Pin 16
GND = Pin 8

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}	
Logic Levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
Active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(10 + 9 = 19)
Active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(carry + 5 + 6 = 1

4 bit adder

74LS367A



hex buffer 4 & 2 bit (tri-state)

PIN OUT FOR DIGITAL BOARD

1–SW1	2–SW2
3–SW3	4 – SW4
5 –SW5	6 –SW6
7 –SW7	8 –SW8
9 –GND	10 – NC
11 –GND	12 – NC
13 –GND	14 – NC
15–GND	16 – NC
17 –LED1	18 –LED2
19 –LED3	20 –LED4
21 –LED5	22 –LED6
23 –LED7	24 –LED8
25 –GND	26 – NC
27 –GND	28 – NC
29 –GND	30 – NC
31 –GND	32 – NC
33 –CLK	34 – NC
35 – NC	36 – NC
37 – NC	38 – PULSE
39 – NC	40 – NC

TO CALCULATE CLOCK FREQUENCY USE THE FOLLOWING FORMULA

$$F = \frac{1.41 \times 10^{-6}}{C}$$

F = frequency

C = capacitor

example : if a 1.0 uF capacitor is used ;

$$F = \frac{1.41 \times 10^{-6}}{1 \times 10^{-6}}$$

F = 1.41 Hz or $\frac{1}{F}$ 0.709 sec.