CS2125 Paper Review Form - Winter 2018

Reviewer: Mike Maksimov

Paper Title: A General Framework for Formalizing UML with Formal Languages

Author(s): William E. McUmber and Betty H.C. Cheng

1) Is the paper technically correct?
 [X] Yes
 [ ] Mostly (minor flaws, but mostly solid)
 [ ] No

2) Originality
 [ ] Very good (very novel, trailblazing work)
 [ ] Good
 [X] Marginal (very incremental)
 [ ] Poor (little or nothing that is new)

3) Technical Depth
 [ ] Very good (comparable to best conference papers)
 [X] Good (comparable to typical conference papers)
 [ ] Marginal depth
 [ ] Little or no depth

4) Impact/Significance
 [ ] Very significant
 [X] Significant
 [ ] Marginal significance.
 [ ] Little or no significance.

5) Presentation
 [ ] Very well written
 [ ] Generally well written
 [X] Readable
 [ ] Needs considerable work
 [ ] Unacceptably bad

6) Overall Rating
 [ ] Strong accept (award quality)
 [X] Accept (high quality - would argue for acceptance)
 [ ] Weak Accept (borderline, but lean towards acceptance)
 [ ] Weak Reject (not sure why this paper was published)

7) Summary of the paper's main contribution and rationale
   for your recommendation. (1-2 paragraphs)

The authors introduce a general framework for formalizing a subset of UML diagrams (class and statechart) into two formal languages, Promela and VHDL. This is achieved by using homomorphic mapping, as well as constructed mapping rules, between UML metamodels and metamodels that describe the target formal language, allowing the preservation of structural relationships between entities. The resulting specifications derived from the UML diagrams enable us to carry out various simulations, as well as analysis through model checking, which are necessary safety critical procedures, especially in the embedded system domain which this paper primarily focused on. The paper concludes by introducing an automated tool (Hydra) for translating UML diagrams into executable specifications, as well as an industrial case study.

I believe that the authors were successful in their development of a framework for formalizing UML with formal languages. Although the support for various types of UML diagrams and specification languages is currently limited, the work presented in the paper still enables various forms of simulation and model checking on UML class diagrams and statecharts. One thing that bothered me as far as paper presentation goes, is the hectic and non-

strategic reference and organization of figures. At times the reader is left to traverse half the paper in order to look at one figure, or prompted to compare two figures which are on the opposite ends of the paper.

8) List 1-3 strengths of the paper. (1-2 sentences each, identified as S1, S2, S3.)

S1 – The framework derived from this paper enables (although limited) structural and behavioral analysis of UML models, which is critical for the design process in most embedded systems. This is achieved by providing methods that formalize UML diagrams into a number of formal languages, allowing simulations and model checking on the outputted specifications.

S2 – The resulting specifications leading from the translation of a UML model into a pre-defined formal language can be used with existing tools that support those languages. This enables developers to continue to use widely accepted development techniques, both in terms of modelling languages as well as the target specification language.

9) List 1-3 weaknesses of the paper (1-2 sentences each, identified as W1, W2, W3.)

W1 – The developed framework only supports a limited set of specification languages (Promela and VHDL), as well as a limited set of UML diagrams (class and statechart).

W2 – The paper did not display (due to space) a more broad set of their developed formalization rules.