Characterization and Parameterized Generation of Digital Circuits

Michael Hutton

Ph.D. Departmental Oral

Department of Computer Science

University of Toronto

Wednesday, March 26, 1997

11am, LP 378

Context and Motivation

Benchmark circuits needed to evaluate and test:

- new FPGA architectures
- new algorithms.

- Some benchmarks exist (PREP, LGSynth, proprietary)

- Hard to find enough and the right size
  - usually big, sometimes specific size range.

➢ Generate synthetic circuits

- learn and use physical properties

Realistic circuits. How?

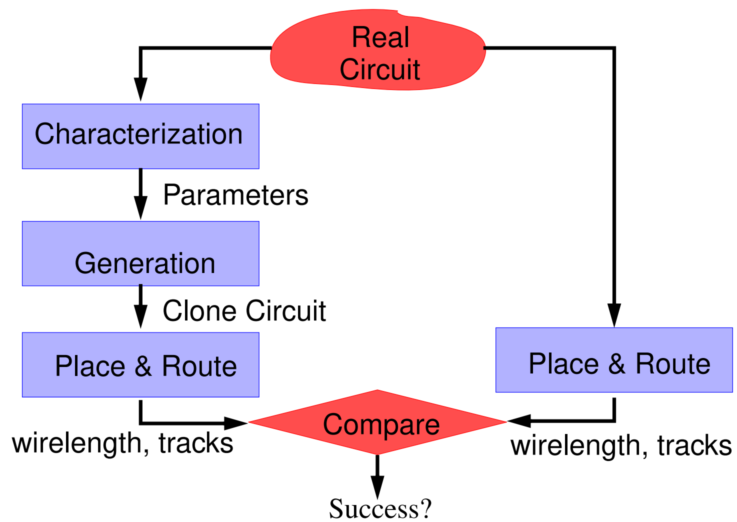
Goal is to generate realistic synthetic circuits.

- *Define* physical characteristics of circuits.
- *Characterize* real circuits for default profile. (CIRC)
- *Generate* circuits from user-parameters and the default profile (GEN).

Validation is crucial!

- Easy to generate random graphs.
- Not easy to generate good synthetic circuits.

Validation Process - A Preview



Previous Efforts

[Donath, Feuer, El Gamal, and others]

- Stochastic wireability analysis, Rent's Rule.

[MCNC, PREP, industry]

- Collect public or private "real" benchmarks.

[Darnauer and Dai]   (independent, parallel work)

- Generate random graphs based on Rent's Rule.

[Iwama et. al.] (independent, parallel work)

- Random logic functions by transformation.

I. Characterizing Combinational Circuits

Combinational Circuit Characteristics

Basic Parameters:

- size, I/O, edges, fanout distribution.

Delay-Based Characteristics:

- delay, shape, edge-length, fanout by level.

Reconvergence:

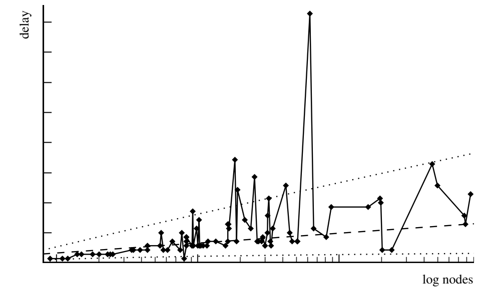
- quantification of reconvergent fanout, R.

Locality:

- spread, average in span (in progress).

Statistical Relationships

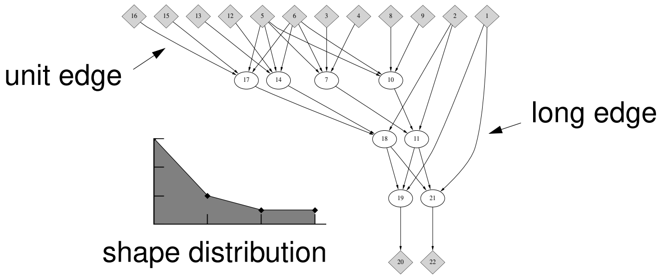
Example: Size vs. combinational delay:

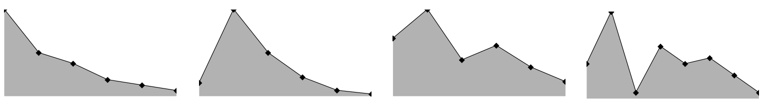


delay = gauss(μ = log(size))

Structural Characteristics

Example: Shape and edge length functions.



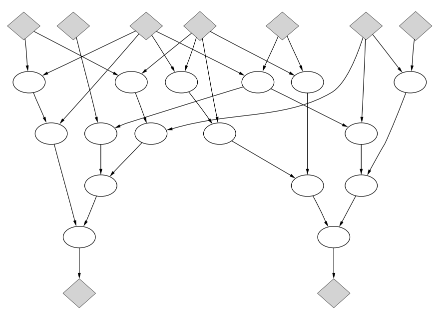


(36/108) (53/108) (12/108) (8/108)

II. Generating Combinational Circuits

Example Characterization / Generation

n=23
k=2
nPI=7
nPO=2
delay=4
shape=(7,6,5,3,2)
fanout=(2,15,3,1,2)
edges=(0,29,3)
locality=6



Important: Algorithm based on delay, shape, fanout.
-- real circuit characteristics.

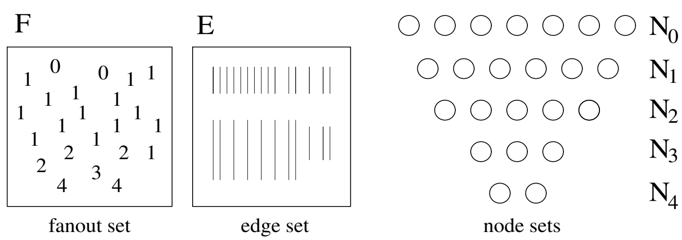
Generation Problem Specification

GIVEN: n, k, nPI, nPO, delay, locality, distributions

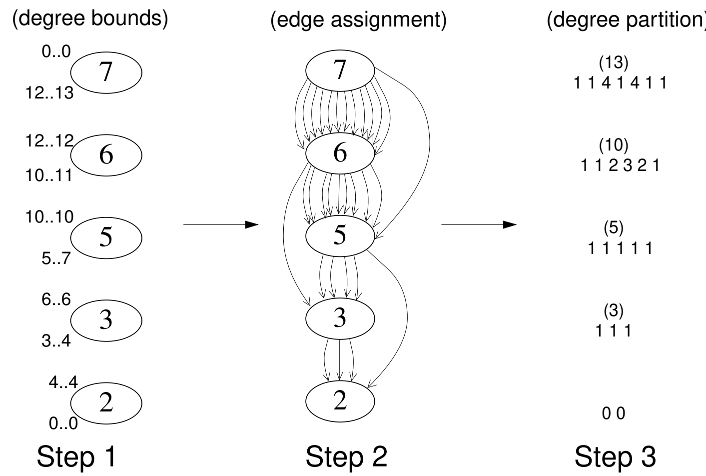
FIND: Circuit C such that:
I. nodes and edges match distributions
II. fanout corresponds to assigned value
III. delay(x) is well-defined for all nodes x
IV. fanin(x) bounded by k, all fanins distinct

Hard and time-consuming optimization problem:
☞ Solve heuristically

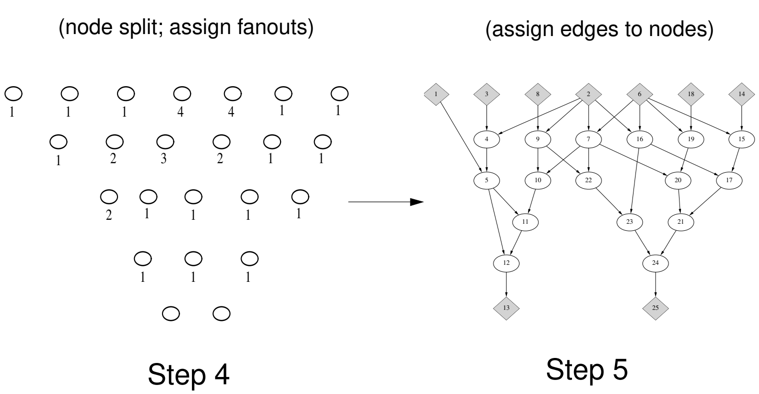
Pictorial Description of the Problem



Combinational Algorithm:

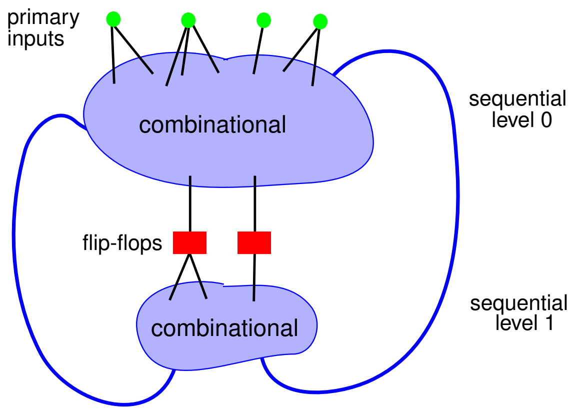


Combinational Algorithm, continued.



III. Sequential Circuits

Modelling Sequential Circuits



Key: combinational sub-circuits are joined by flip-flops and back-edges.

Sequential Circuit Characteristics

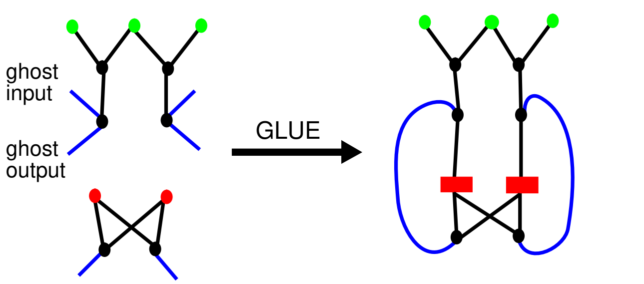
New Characteristics

- sequential level, sequential shape
- forward edge, back edge, FF-edge
- nDFF, nBack
- delay locations of back edges

“Ghost I/O ports”

- at head and tail of back-edges
- have a shape distribution (important)

Sequential Generation Algorithm



(POs not shown)

Basic Approach:

1. Combinational sub-circuits (many new constraints).
2. Glue sub-circuits: iterative, greedy algorithm.

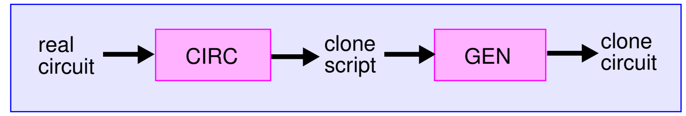
The Gluing Process

- Previously had *combinational delay* and shape.
  - add *sequential level*, shape, “ghost” I/Os.
- Input at sequential level >0 becomes a FF in gluing.
- Introduce ghost input (GI) and output (GO) ports:
  - abstractly like a PI or PO in a sub-circuit, but disappear in gluing.
  - have delay-locations: GIshape and GOshape
  - GI and GO must be delay-compatible to join.

Note: the model generalizes to arbitrary hierarchy.

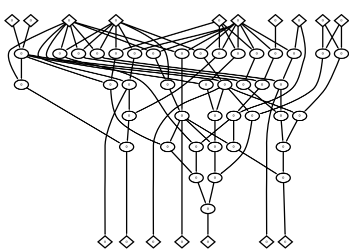
IV. Validation of Circuit Quality

GEN-scripts and “Clone” Circuits

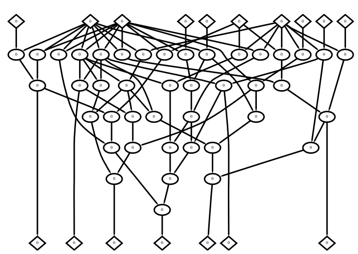



```
X = {
  name = “bbtasclone”;
  L0=(@.comb_circ) {
    name=”L0”; n=8; kin=4; nPI=2; nPO=2;
    nDFF=0; nEdges=7; level=0; delay=2; nBot=3; shape=(2,3,3);
    nGI=13; GIshape=(4,9,0); nGO=3; GOshape=(0,0,3); nZeros=5;
    POshape=(0,2,0); edges=(0,7,0); outs=(5,0,2,1); max_out=3
  };
  L1=(@.comb_circ) {
    name=”L1”; n=3; kin=4; nPI=0; nPO=0;
    nDFF=3; nEdges=0; level=1; delay=0; nBot=3; shape=(3);
    nGI=0; GIshape=(0); nGO=13; GOshape=(13); nZeros=3;
    POshape=(0); edges=(0); outs=(3); max_out=0;
  };
   glue=(L0,L1);
};
output(circuit(X));
```


Combinational Circuit Clone

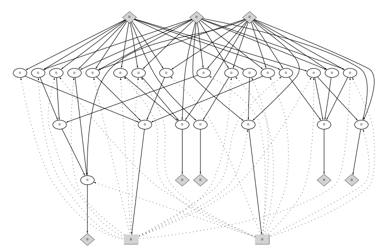


MCNC circuit x2

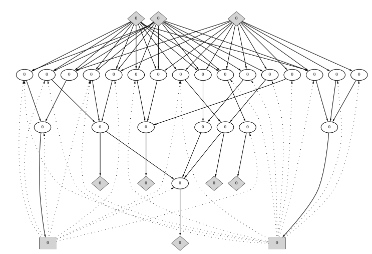


GEN clone of x2

Sequential Circuit Clone

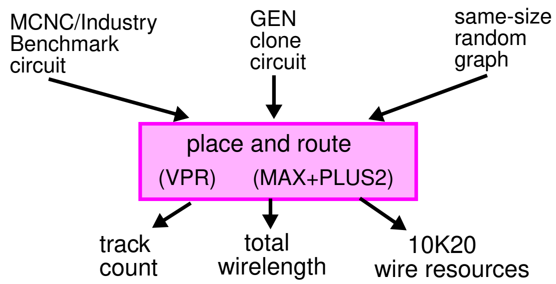


MCNC circuit dk15



GEN clone of dk15

Validation of Routability



Compare real circuits against GEN-clones and “random” graphs with same #nodes and edges.

Note: We use very fair and reasonable random graphs.

Results for Combinational Circuits

	size	Reconvergence MCNC	Reconvergence GEN	Reconvergence RAND	Tracks MCNC	Tracks GEN	Tracks RAND	Wirelength MCNC	Wirelength GEN	Wirelength RAND
[illegible]	500	0.78	0.86	0.29	8	7	15	5612	5019	9159
x3	512	0.26	0.24	0.08	4	5	10	3454	4299	7029
ex4p	514	0.41	0.25	0.24	4	5	12	3425	3914	8604
apex6	528	0.25	0.21	0.08	4	6	10	3217	4431	7116
C6288	559	0.90	1.16	0.45	4	8	16	2900	6207	10287
k2	559	0.60	0.60	0.13	7	7	14	5190	5151	9139
misex3c	564	0.54	0.64	0.37	6	5	15	4941	4454	10989
dalu	575	0.46	0.49	0.19	5	6	13	3827	4971	9547
i8	614	0.77	0.43	0.13	5	7	15	5729	6451	10181
apex1	740	0.67	0.56	0.36	8	7	19	8124	7725	15226
apex3	921	0.66	0.59	0.30	8	7	19	10658	9831	34424
C7552	945	0.54	0.45	0.05	5	6	13	5751	10494	15918
ex5p	1072	1.12	1.20	0.27	10	8	21	14443	12615	27904
i10	1252	0.72	0.55	0.09	6	8	19	15095	24915	28738
apex4	1270	0.90	0.69	0.24	9	8	23	16412	14279	34424
misex3	1411	0.55	0.77	0.34	8	7	24	16139	14799	40152
alu4	1525	0.50	0.62	0.22	7	6	26	15818	13561	45177
seq	1791	0.49	0.67	0.21	8	7	27	21349	19796	57040
des	1847	0.50	0.39	0.07	6	9	23	17959	23925	50294
apex2	1916	0.47	0.64	0.20	8	8	29	24203	22742	64418
spla	3706	0.97	1.07	0.13	10	9	19	49734	62584	167842
pdc	4591	1.01	1.27	0.10	11	10	19	74654	66131	226679
signed difference			9%	-46%		3%	123%		10%	119%
absolute difference			22%	49%		14%	123%		17%	119%

(MCNC benchmarks)

Wirelength	GEN: 17%	RAND: 119%
Track Count	GEN: 14%	RAND: 123%
Reconvergence	GEN: 22%	RAND: 48%

Results for Sequential Circuits

Circuit	VPR wire orig	VPR wire clone %diff	VPR wire rand %diff	VPR tracks orig	VPR tracks clone %diff	VPR tracks rand %diff	10K20 tracks clone %diff	10K20 tracks rand %diff
A	5102	21	144	6	16	83	14	132
B	7719	64	215	5	80	160	71	.
C	6344	27	160	6	16	116	30	.
D	6818	20	147	6	16	133	32	.
E	6609	53	266	5	60	160	35	.
F	4293	57	188	5	40	140	41	197
G	4147	2	158	5	0	140	16	208
H	5107	21	137	5	40	120	0	123
I	4692	19	155	5	40	160	23	132
J	6087	34	153	5	60	120	51	165
K	9313	42	202	6	33	133	38	.
L	6546	36	222	6	33	100	55	.
M	7748	86	248	5	100	220	85	.
N	10794	-43	52	10	-40	30	-41	.
O	8070	17	140	7	14	100	25	.
P	5562	88	268	5	80	180	90	.
Q	6460	71	167	5	80	160	.	.
S	6417	29	166	5	40	140	24	.
T	4662	28	170	6	0	83	16	108
U	8828	2	156	6	16	150	53	.
V	4876	81	201	4	75	175	63	174
W	4837	28	143	4	50	150	34	117
mean	6358	35%	175%	5.5	38%	134%	36%	151%

(Altera benchmarks)

Wirelength:
GEN: 35%
RAND: 175%

Track Count:
GEN: 38%
RAND: 134%

10K20 “wires”:
GEN: 36% (1 fail)
RAND: 151% (13 fail)

(real circuits all fit)

V. Conclusions and Future Work

Why This Work is Important

Heuristic solutions *must* understand input data.

- We provide new characteristics of digital netlists, useful both for this problem and CAD in general.
- Heuristic algorithm increasingly important.

Benchmarks are necessary but rare.

- We describe a *new*, *viable* and *practical* approach to generating benchmarks.
- Based on known aspects of circuits (e.g. delay).

Test data must be *believable*.

- We give a concrete approach to validation, and show conclusively good results.

Specific Contributions of This Thesis

- New characteristics of combinational circuits: shape, edge length, POshape, reconvergence, locality.
- New abstract model for sequential and hierarchical circuits: GI and GO shape, gluing.
- Define circuit generation problem and requirements for solution. Give an algorithmic solution, implementation, and empirical validation.
- Practical research tools for future work and the industrial community.

Users of CIRC and GEN software.

Actel	Motorola
Altera	Northern Telecom
AMD	Pilkington
Cypress	Sierra Imaging
Hewlett Packard	Synopsys
Mentor Graphics	Vantis
MINC	Xilinx

Also 25 academic or individual users.

1996 DAC partitioning contest.

(accepted licencing criteria and downloaded software)

Future Work

For implementation in GEN:

- Fine tune parameters, more and varied circuits
- New netlist formats, stitching, LUT functionality.

Further Research:

- Better understanding and handling of “locality.”
- Better understanding of circuit structure with size.
- Hierarchical and “system” level generation.
- Validating large circuits?
- Validation for partitioning, logic synthesis, simulation, power consumption.